Designing a Workflow for Printed Electronics with Open Source Software

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By

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On my honor as a University student, I have neither given nor received unauthorized aid on this assignment as defined by the Honor Guidelines for Thesis-Related Assignments.

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ABSTRACT

One of the biggest benefits of printed electronics is the rapid and cost effective prototyping it can offer compared to traditional fabrication methods. As such, the research project aimed at creating a layout-to-print workflow involving open source software, further avoiding costs of expensive design software. The Organic Process Design Kit, from the University of Minnesota, was implemented within the open source Electric VLSI Design System. The layout was exported, converted, and imported to the materials printer's software to be printed. The workflow was capable of producing a final printed circuit designed from scratch, with a few errors to be addressed in future research.

INTRODUCTION

Today, there is much research and work looking into the field of printable electronics. According to Perelaer et al. (2010), printable electronics is "a highly viable and innovative fusion of three technological areas — microelectronics, chemistry and printing" (p. 8446). As such, printable electronics is predicted to become a significant industrial force. Printable electronics is the printing of various circuitry and organic LED's on common substrates such as paper and plastic using a specialized inkjet printer. Much different electronic architectures have been created in printed electronics, such as flexible batteries, logical memory components, and field-effect transistors. More complex structures are in the works as well. Through their research, Kim et al. (2013) has noted that electrolyte-gated transistors work very well in printed circuits and can act as backing for rollable, or flexible, displays, which can be used in applications such as bio sensing. Other researchers, Keskinen et al. (2012), have developed supercapacitors that

make memory logic in printed circuits a closer reality. There is a great deal of possibilities for research in printed electronics.

As with any new technology, there is some doubt as to the effectiveness and utility of printed electronics. However, many tests reveal that the use printed electronics is highly feasible. Authors Öhlund, Örtegren, Forsberg, and Nilsson (2012) believe that "the widespread usage of paper and board offer largely unexploited possibilities for printed electronics applications" (p. 731). Through their tests, they found that porosity and roughness of the surface of the substrate could impact the reliability of a printed circuit significantly. Addressing this issue, Denneulin, Bras, Blayo, and Neuman (2011) developed "a UV-curing inkjettable primer layer" (p. 3645). The printed circuits performed significantly better when printed on a paper substrate that was pre-treated with their primer. This development made the usage of printed circuits to make interactive labels and advertisements more feasible.

Because of the ability to be printed on readily available substrates (as opposed to silicon), one of the biggest appeals of printable electronics is more cost efficient prototyping. As explained by Kunnari, Valkama, Keskinen, and Mansikkamäki (2009), "traditional electronics is cheap only on the mass-production scale" whereas the printed electronics are "flexible and cheap… for tailored small-volume products" (p. 791). Instead of needing millions of dollars of micro fabrication machinery to manufacture a circuit that may or may not be desirable, designers are able to use a relatively cheaper printer to print an instance of the circuit on paper for functionality testing. Economics is just one benefit of printed circuitry.

The research project aimed at furthering the cost effectiveness of printed electronics and laid some groundwork for future research into printed electronics at the University of Virginia. Specifically, the goal was to implement an Organic Process Design Kit (OPDK), a PDK

designed to be used in the Cadence Virtuoso design environment, in an alternative open source design environment. Cadence licensing can be very expensive, diminishing the benefits of cheaper prototyping that can be obtained from printed electronics. As a result of this cost, the research sought to create an alternative workflow, starting from layout in open source software and ending in a final printed circuit from the materials printer.

APPROACH

At the start of the research, it was important to determine what parts would be needed to implement a fully functioning workflow from layout to final printed circuit. The Organic Process Design Kit was selected as the PDK to be used in the layout designs. Next, the Electric VLSI design system was chosen as the open source layout software to be used in the workflow. Lastly, the layout design was to be sent to the University of Virginia's electronics printer, the Fujifilm Dimatix Materials Printer 2800 (DMP-2800). This is a brief overview of our approached. The individual sections are described in the forthcoming sections.

Organic Process Design Kit (OPDK)

The OPDK was created in the University of Minnesota and designed to fully facilitate the entire design of organic thin-film transistors (OTFT). Organic thin-film transistors are ideal for printing, but have always relied on post-printed examination for verification of designs. Layouts can now be drawn for organic transistors with verification introduced by the OPDK's DRC. While originally designed to be used with the Cadence Virtuoso design environment, our research was centered on translating or implementing the OPDK within open source software, specifically the Electric VLSI design system.

Our research started in understanding the OPDK and how its OTFTs functioned. The first step taken was to work through the user manual as well as tutorials distributed by the University of Michigan alongside the OPDK. Carefully walking through the documents allowed us to list and understand the purpose of the important layers that would be eventually implemented in the alternative design software.

Eventually, we deemed the PDK feasible for our purposes. The OTFTs were created by laying out metal electrodes to act as a source and drain. Then, a P3HT layer is printed across the electrodes to connect them and act as the channel. Next, an ion-gel dielectric is laid on top of the channel. The ions within this gel act as the carriers to allow current to conduct through the channel. Lastly, a PEDOT conductive layer is laid on top of the ion gel to act as the gate. The simplicity of this layered design made the P3HT OTFTs ideal for printed electronics. With the OPDK selected, the next step was to find suitable open source design software.

Electric VLSI Design System

The open source software that we have concentrated on is the Electric VLSI design system from Static Free Software. Electric is a versatile program written in JAVA and provides many features needed to design and layout at no cost. Electric gives users the ability to create and implement custom technologies, design schematics, and draw layouts that can be exported in a multitude of formats. The program also offers more advanced features that may be desirable to future research in printed electronics, such as three-dimensional layouts.

As the program is free and provides many of the utilities and design needs that Cadence Virtuoso does, we decided to use it in the proposed workflow. Once a layout had been drawn with the OPDK and Electric design tool, the next logical step was to send the layout to the materials printer software.

Fujifilm Dimatix Materials Printer (DMP-2800)

The Dimatix Materials Printer along with its respective software, the Dimatix Drop Manager, is capable of receiving a few different formats of layout. Upon importing supported layout formats into the software, such as BMP or GERBER, the layout can quickly be converted to a format received by the materials printer. The printer can accept cartridges of various materials that allow us to print circuits on paper, film, or other thin substrates. The goal of our research was to successfully print a circuit that we had designed from scratch, demonstrating a successful start-to-finish workflow.

FINAL PROPOSED WORKFLOW

Ultimately, the research project met success in developing a workflow. Other than a few steps added as needed to the original approach, the core of the workflow is very similar to our original proposal.

Layout in Electric VLSI Design System

In the early stages of the research, the important layers of the OPDK was implemented within the Electric program, albeit elementarily. Because it was appealing to keep things simple and worry about refinement later, the original DRC of the OPDK was not fully implemented.

The research project was meant to focus more on moving a layout from design to print. Thus, the OPDK technology library created in Electric has very minimal DRC rules that will be augmented in future research.

As the layers are now implemented in Electric, the first step of the proposed workflow can be completed. Using the created technology file, we were able to design a layout using our custom layers. Then, we exported the layout from Electric. For our purposes, we chose to export the layout in the SVG file format (Scalable Vector Graphics).

Convert SVG to BMP

The SVG file format unfortunately was not compatible with the Dimatix software. Therefore, a conversion from SVG to BMP was needed. A conversion such as this can be done with many different image-processing software. A free online converter was used. While a more in-depth program will be sought out for our workflow in the future, this online converter would suffice as it allowed us to specify dimensions and DPI of the converted BMP.

Alter BMP Bit Depth

After obtaining our BMP, it was necessary to reduce the bit depth from 8 to 1. Bit depth refers to the color bits used to specify the color of each dot or pixel. The Dimatix software is capable of importing only 1 bit BMP. Essentially, this meant that the printer would only interpret a pixel as a 0 or a 1 (leave blank or print a drop of ink). This reduction in bit depth was fairly difficult to accomplish. Eventually an image-processing program, ImageMagick, was used to successfully convert the BMP to a monochrome (1 bit depth) BMP. After this conversion, the monochrome BMP was able to be imported to the Dimatix software.

Design to Dimatix Drop Manager

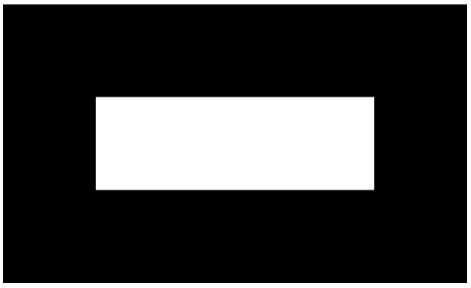
At this stage in the design workflow, all that was left was the actual printing. The converted monochrome BMP described in the above section was imported into the Dimatix Drop Manger software and turned into a pattern (.ptn) file. This .ptn file is the format that the printer can actually interpret for printing. Then, it was straightforward to print the pattern onto the photopaper.

RESULTS

The final prints of our original layout showed a few desired features, while also revealing issues that would need to be addressed in future work.

The Designs

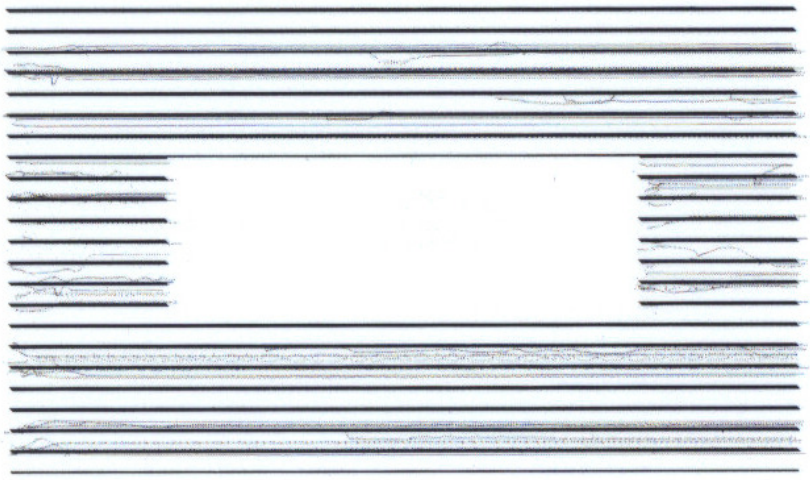
The original layout designed in the Electric VLSI design system appears as follows (the layout may appear fuzzy as it was enlarged a great amount to be visible):



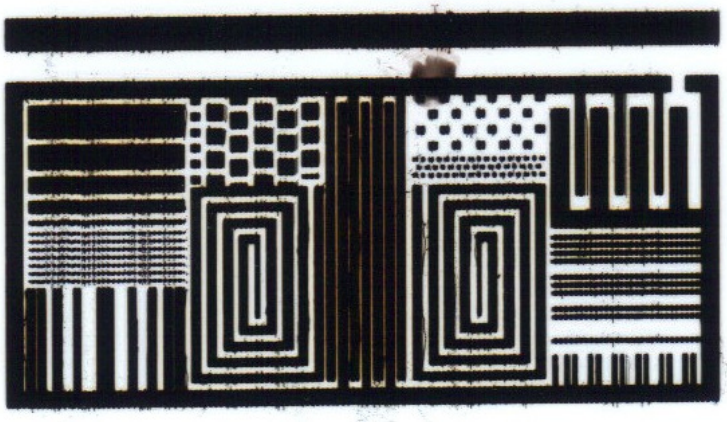
Within the Electric software, this rectangle (left) was designed with an overall length of 5 cm, and a width of 3 cm. The empty rectangle (white) inside was 1 cm by 3 cm. To clarify, the blue is where material should be deposited by the printer, and the white is to be left blank. Upon converting the image to monochrome, the only notable difference is that the image turns purely black and white (right).

The Prints

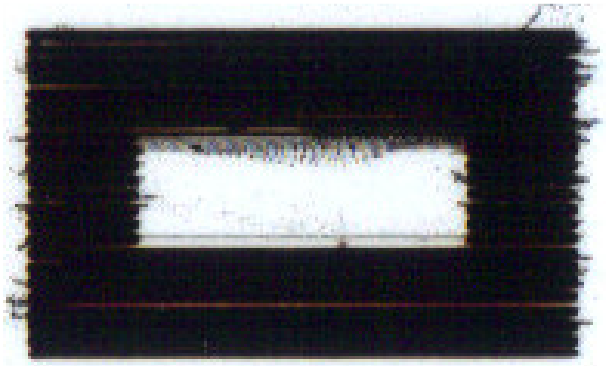
Two different prints were completed to test the design to print portion of the workflow. Both prints had different desirable qualities, as well as issues to be resolved in future work. The first print is shown below:



The first print met the exact design dimensions of 3 cm by 5 cm and is representative of our original intended design. However, the print was odd and appeared as if the printer only printed every fifth line or so. The rectangle should appear solid. It can be said confidently that the issue in the print does not lie in the printer's resolution limit, as the printer was able to print the following test image of roughly the same dimensions, appearing much more solid:



In an attempt to create a much more solid print of the same design layout, the DPI was increased by a factor of approximately three (from 300 DPI to 1016 DPI). The second print is shown below:



While the design did indeed become more solid, the increased DPI created a new problem. The print was a lot smaller, measuring at approximately 1 cm by 1.5 cm. The second print was also representative of the original intended design, but was smaller than designed.

CONCLUSIONS

Through the results obtained from the final proposed walkthrough, it is clear that the use of our workflow to print circuit designs is indeed feasible. While the final obtained prints were either low resolution (not solid) or too small, the shapes are indicative that the workflow does work from a layout-to-print perspective. What the workflow needs now to become more successful is refinement. It is suspected that both of the problems with the prints – resolution and sizing – can be addressed when exporting the layout from Electric and when converting from SVG to BMP. At both of these steps, the user is given the opportunity to make adjustments to resolution and DPI. With more time and experimentation, our research could find how to adjust these values accordingly to achieve a high DPI print that appears solid and maintains original design dimensions.

FUTURE WORK

There are several objectives and refinements that the research project could continue into, given more time. The first of which is adding more comprehensive DRC into the OPDK technology implemented in Electric. As is, there is very little DRC in the technology file. However, the original OPDK from the University of Minnesota provides their DRC lists, so a translation would be feasible.

At the SVG to BMP conversion step, it would be a good idea to try to figure out how to complete this conversion with ImageMagick instead of an online converter. This way, the workflow would only have one intermediate program (ImageMagick) to both convert from SVG to BMP as well as convert the resulting BMP to a 1 bit depth BMP, perhaps even in one combined step. ImageMagick is the only method found to successfully change a BMP to a bit depth of 1.

When exporting layout from Electric, it would be beneficial to test a few different formats that are known to be compatible with the DMP-2800 printer. Time was limited, but the printer is also able to accept GERBER format, which Electric is capable of exporting.

As mentioned in the conclusion, the workflow also needs to be refined to output quality prints at the exact specified design dimensions. There are many different interconnected programs used in the workflow, so there is a multitude of variables that will make this particular refinement difficult and time-consuming.

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